REMARKS

Claims 1, 10, 19, 28, 34, 45, 51, 57, and 59 have been amended. Claim 60 has been canceled. No new claims have been added. Hence, claims 1-59 are pending.

Claims 10, 28, and 45 stand objected to due to informalities. Claims 10, 28, and 45 have been amended. Accordingly, the objection to claims 10, 28, and 45 should be withdrawn.

Claims 1-15, 18, 34-38, 41-50, and 57-60 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kondo (U.S. Patent No. 6,539,444) in view of Frame (U.S. Patent No. 5,349,690). Claims 16-17, 19-33, and 39-40 stand rejected under 35 U.S.C. § 103(a) over Kondo, Frame, and Nguyen (U.S. Patent 5,502,821). Claims 51-52 and 55-56 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kondo and Nguyen. Claims 53-54 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kondo, Nguyen, and Singh (U.S. Patent No. 6,609,171). These rejections are respectfully traversed.

Each independent claim recites the use of a link bus hub for a link bus comprising a plurality of link bus segments. More specifically: Claim 1 recites, *inter alia,*

> A bus arbitration method for ... system comprising a hub device for a link bus comprising a plurality of link bus segments, said hub device coupled to a processor by a processor bus and coupled to a memory device by a memory bus, said hub device being connected to a first device by <u>one of said</u> link bus <u>segments,</u> said method comprising the steps of: issuing, from one of the first device and the hub device, ...; determining, at the first device and the hub device, ...; and ..., wherein control of the link bus is granted by the first device and the hub device.

Claim 19 recites, *inter alia,*

> A method of arbitrating control of a link bus comprising a plurality of link bus segments in a computer system, the computer system comprising a hub device for the plurality of link bus segments, said hub device coupled to a processor by a processor bus and coupled to a memory device by a memory bus, the hub device being connected to a satellite device by one of the link bus segments, ... said method comprising the steps of: time-multiplexing, from one of the satellite device and the hub device, ...; detecting, at the other of the satellite device and the hub device, ... wherein control of the link bus is granted by the satellite device and the hub device.

Claim 34 recites, *inter alia,*

> A processor system comprising: ... a link hub for a link bus, said link bus comprising a plurality of link bus segments each coupled to said link hub, said link hub also connected to said processor via a processor bus; ... one of said link bus segments being connected between said link hub and said satellite device, wherein said satellite device and said link hub arbitrate a control of said link bus by issuing, ... an arbitration request ..., determining, ... whether control of said link bus can be transferred from a bus master to the device issuing the arbitration request, and transferring control of said link bus from the bus master to the device issuing the arbitration request.

Claim 51 recites, *inter alia,*

> A processor based system comprising: a processor; a link hub for a link bus comprising a plurality of link bus segments each coupled to said link hub, said link hub also connected to said processor by a first bus; ... one of said link bus segments being connected between said link hub and said satellite device.

And claim 57 recites, *inter alia,*

> A processor based system comprising: ... a link bus hub for a link bus comprising a plurality of link bus segments each connected to said link bus hub, said link bus hub also connected to said processor by a first bus; ... wherein one of said link bus segments is connected between

> said link bus hub and said first device, comprises a source strobed command/address/data bus, two clock strobes and a link bus status line, and supports a link bus protocol wherein said link bus hub and said second device arbitrate control over said link bus in a decentralized manner and in accordance with said link bus protocol such that control over said link bus is transferred from a bus master to a bus slave when the slave is granted control over said bus.

Kondo is directed to an information processing apparatus having a plurality of buses. The Office Action alleges that Kondo discloses the link bus hub and link bus of the independent claims. More specifically, the Office Action alleges that in Fig. 12, the bus adapter 4 is equivalent to the claimed link bus hub, and the system bus is equivalent to the claimed link bus. However, each of the independent claim requires the link bus to be comprised of a plurality of link bus segments. Further, each link bus segment is required to be coupled to the link bus hub. It is respectfully submitted that all Fig. 12 shows is a bus adapter 4 which operates as a conventional mulit-way a bus bridge between the processor bus 3, memory bus 11, and system bus 5. There is no teaching or suggestion in Kondo regarding a link bus comprising multiple link bus segments each coupled to a link bus hub. None of the buses 3, 11, and 5 of Fig. 12 comprise multiple segments which are coupled at any sort of hub device. Accordingly, Kondo fails to teach or suggest the above quoted limitations from each of the independent claims.

The Office Action additionally cites to Frame, Nguyen, and Singh. However, these references, like Kondo, also fail to teach or disclose the claimed link bus, plurality of link bus segments, and a link bus hub coupled to each of the link bus segments. None of the recited prior art, whether taken individually or in combination, teaches or suggests the above quoted limitations from the independent claims.

Accordingly, independent claims 1, 19, 34, 51, and 57 are believed to be allowable over the prior art of record. The depending claims (2-18, 20-33, 35-50, 52-56,

and 58-59) are also believed to be allowable for at least the same reason as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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